IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
BARRET

Serial No.: Herewith

Filed: Herewith

For: CONTROL OF THE ACCESS TO A MEMORY INTEGRATED WITH A MICROPROCESSOR

Group Art Unit: TBA
Examiner: TBA

Commissioner of Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to examination of the above-captioned application, please amend the same as follows:

IN THE CLAIMS

Please replace claims 1, 8, 9, 11 and 12 with the following claims:

1.(AMENDED) A method for controlling the access to all or part of the content of a first memory (2, 3) integrated with a microprocessor (10), comprising:

using a priority-holding interrupt (PRIORIN);

using at least one register of keys (21); and

applying at least one access control algorithm contained in a second auxiliary memory (20) and using the content of at least one also integrated storage element (2) and the

content of the key register, the content of the auxiliary memory being programmable only once.

8.(AMENDED) A circuit comprising a microprocessor (10) integrated with at least one first memory (2, 3), which includes a second auxiliary memory (20) adapted to containing at least one sub-program enabling authorizing the execution of a function of access to said first memory (2, 3), said auxiliary memory (20) being programmable only once.

9.(AMENDED) The circuit of claim 8, further including means (22) for selecting, at the input of a memory interface (14) of the microprocessor (10), a memory from among at least:

said auxiliary memory (20); and

said first memory (2, 3), the selection of said first memory, otherwise than for the execution of a function that it contains, requiring an authorization from an algorithm contained in the auxiliary memory and using the content of at least one also integrated storage element (2) and the content of the key register.

11.(AMENDED) The circuit of claim 8, further including means (24) for generating a priority-holding interrupt for executing said sub-program, the generation occurring provided that:

a signal (MODE) indicative of an access-control-operating mode is in an active state;

an access to the first memory (2) has been requested otherwise than for a non-interruptible execution of one of the functions that it contains; and

an interrupt signal (EXTPRIORIN, INTPRIORIN) is active, the resulting priority-holding interrupt being non-interruptible, even by itself.

12.(AMENDED) The circuit of claim 8, further including means for implementing access to all or part of a content of the first memory (2, 3) integrated with the microprocessor, using a priority-holding interrupt (PRIORIN) and at least one register of keys (21), and applying at least one access control algorithm of at least one also integrated storage element (2) and the content of the key register, the content of the auxiliary memory being programmable only once.

REMARKS

Pursuant to 37 CFR § 1.121, a "VERSION WITH MARKINGS TO SHOW CHANGES MADE" is enclosed, following these remarks.

Claims 1-12 are pending in the application.

Claims 1, 8, 9, 11 and 12 have been amended to conform them to U.S. practice. Claim 12 has been further amended to eliminate the multiple dependencies recited therein.

No fees are believed due as a result of this Preliminary Amendment. The Commissioner is hereby authorized to charge any other fees which may be required, or credit any overpayment, to Deposit Account number 04-1679.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

The following marked-up claims correspond to the replacement claims of this amendment.

1.(AMENDED) A method for controlling the access to all or part of the content of a first memory (2, 3) integrated with a microprocessor (10), [consisting of] comprising:

using a priority-holding interrupt (PRIORIN);

using at least one register of keys (21); and

applying at least one access control algorithm contained in a second auxiliary memory (20) and using the content of at least one also integrated storage element (2) and the content of the key register, the content of the auxiliary memory being programmable only once.

8.(AMENDED) A circuit [integrating] comprising a microprocessor (10) [and] integrated with at least one first memory (2, 3), which includes a second auxiliary memory (20) adapted to containing at least one sub-program enabling authorizing the execution of a function of access to said first memory (2, 3), said auxiliary memory (20) being programmable only once.

9.(AMENDED) The circuit of claim 8, further including means (22) for selecting, at the input of a memory interface (14) of the microprocessor (10), a memory from among at least:

said auxiliary memory (20); and

said first memory (2, 3), the selection of said first memory, otherwise than for the execution of a function that it contains, requiring an authorization from an

algorithm contained in the auxiliary memory and using the content of at least one also integrated storage element (2) and the content of the key register.

11.(AMENDED) The circuit of claim 8, <u>further</u> including means (24) for generating a priority-holding interrupt for executing said sub-program, the generation occurring provided that:

a signal (MODE) indicative of an access-control-operating mode is in an active state;

an access to the first memory (2) has been requested otherwise than for a non-interruptible execution of one of the functions that it contains; and

an interrupt signal (EXTPRIORIN, INTPRIORIN) is active, the resulting priority-holding interrupt being non-interruptible, even by itself.

12.(AMENDED) The circuit of claim 8, <u>further</u> including means for implementing [the] access [control method of any of claims 1 to 7] <u>to all or part of a content of the first memory (2, 3) integrated with the microprocessor, using a priority-holding interrupt (PRIORIN) and at least one register of keys (21), and applying at least one access control algorithm of at least one also integrated storage element (2) and the content of the key register, the content of the auxiliary memory being programmable only once</u>.

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